

FIG. 1

FIRST PRINCIPLE OF PRESENT INVENTION

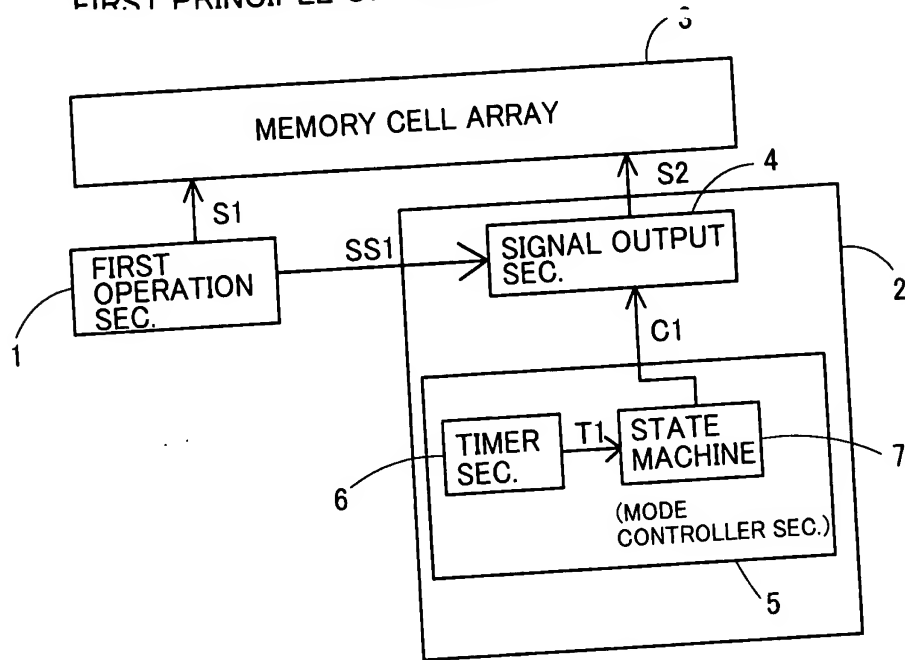


FIG. 2

SECOND PRINCIPLE OF PRESENT INVENTION

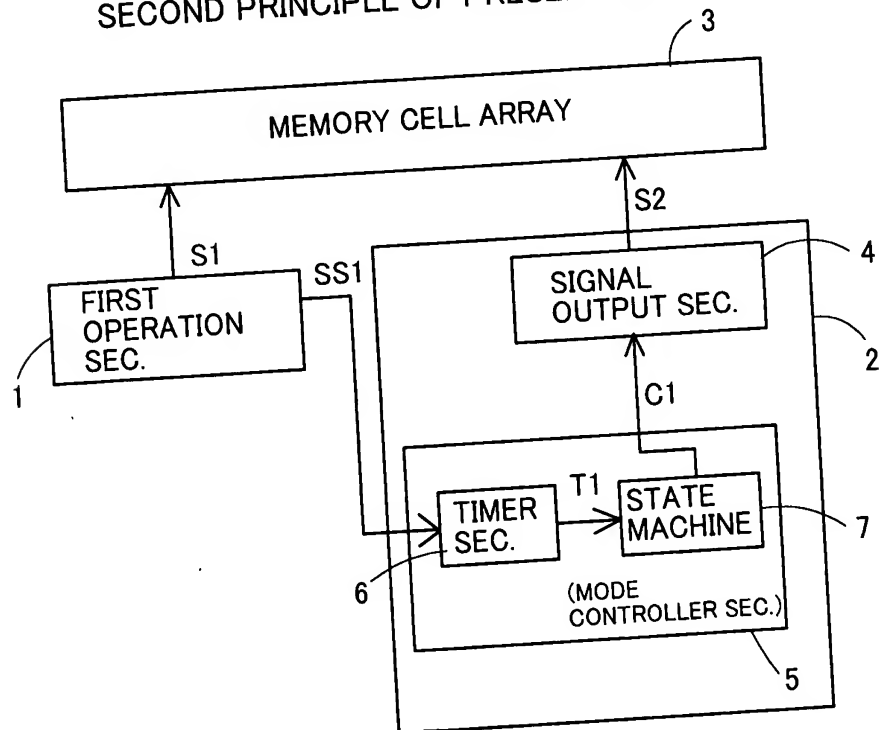
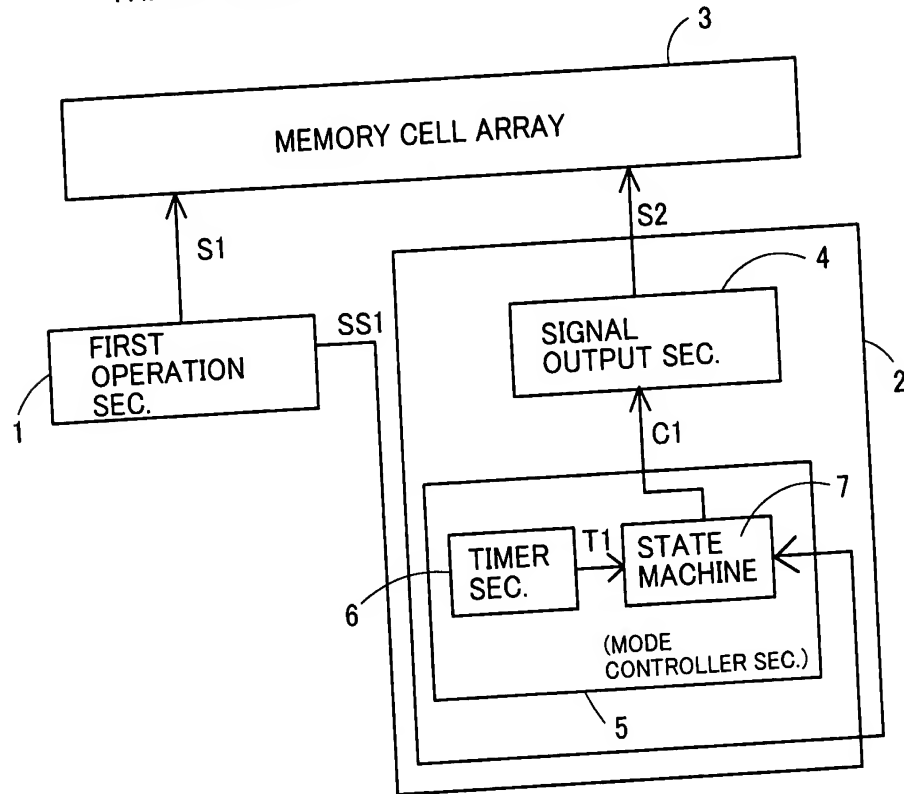


FIG. 3

THIRD PRINCIPLE OF PRESENT INVENTION



The diagram illustrates a semiconductor device with two memory arrays, **BO** and **BN**, and their associated control and sense amplifiers.

**Memory Array BO:**

- 110:** WELL VOLTAGE SWITCH CIRCUIT, controlled by **EOWE**.
- 120:** WORD LINE VOLTAGE SWITCH CIRCUIT, controlled by **EOWL+** and **EOWL-**.
- 140:** READ BIT LINE SWITCH CIRCUIT.
- 130:** WRITE BIT LINE SWITCH CIRCUIT, controlled by **EOWB**.

**Memory Array BN:**

- 11N:** WELL VOLTAGE SWITCH CIRCUIT, controlled by **ENWE**.
- 12N:** WORD LINE VOLTAGE SWITCH CIRCUIT, controlled by **ENWL+** and **ENWL-**.
- 14N:** READ BIT LINE SWITCH CIRCUIT.
- 13N:** WRITE BIT LINE SWITCH CIRCUIT, controlled by **ENWB**.

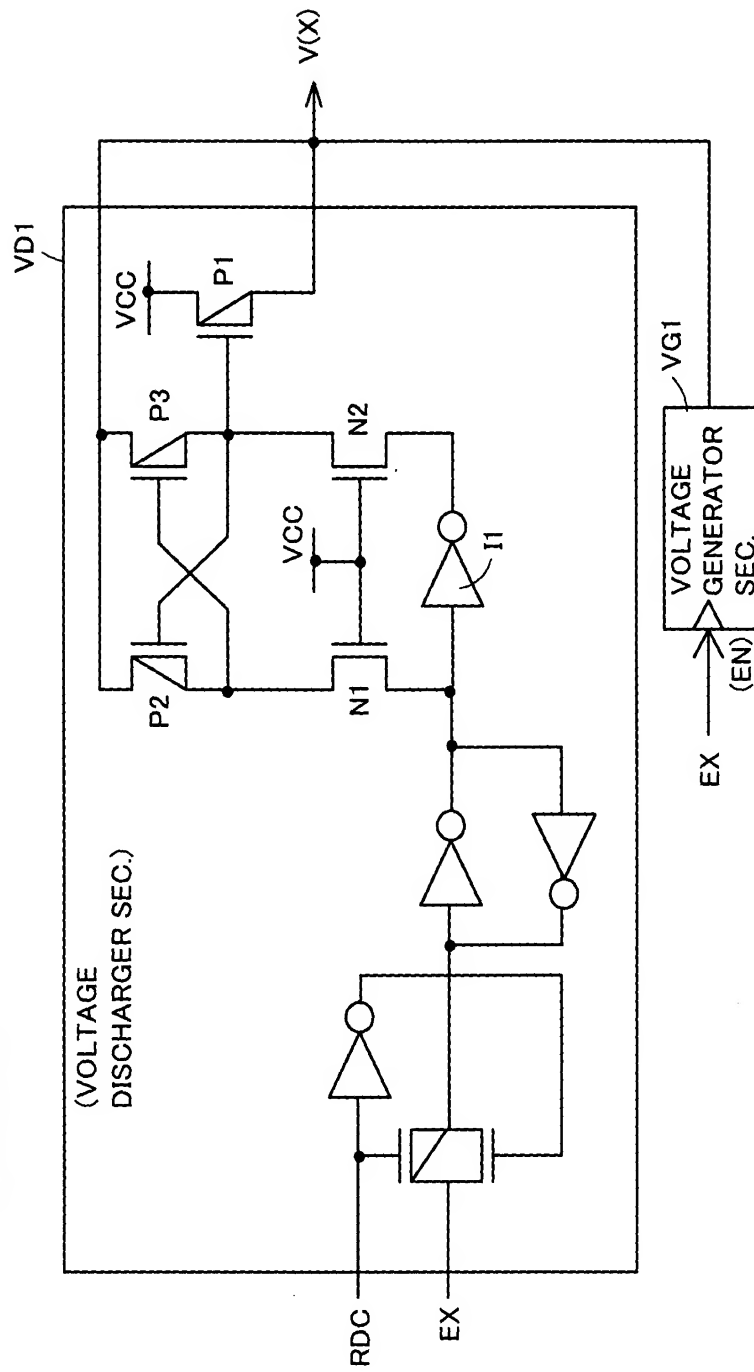
**Control and Sense Amplifier Section:**

- 109:** REFERENCE CELL.
- 108:** SENSE AMPLIFIER, receiving inputs from the read bit line switch circuits (140, 14N) and the reference cell (109). It has control inputs **EQ** and **LT**.
- 17:** (READ CONTROL CIRCUIT) containing:
  - ADDRESS TRANSITION DETECTOR CIRCUIT:** Receives **ADD** and **ATD** signals.
  - PULSE GENERATOR (1):** Receives **ATD** signal.
  - PULSE GENERATOR (2):** Receives **ATD** signal.
- 105:** WRITE CONTROL CIRCUIT, receiving **MODE** and **EX** signals.
- 16:** A set of voltage generator circuits:
  - 16A:** WRITE BIT LINE VOLTAGE GENERATOR CIRCUIT, controlled by **EnX**.
  - 16B:** WORD LINE VOLTAGE GENERATOR CIRCUIT.
  - 16C:** NEGATIVE WORD LINE VOLTAGE GENERATOR CIRCUIT.
  - 16D:** WELL VOLTAGE GENERATOR CIRCUIT.

**Legend:**

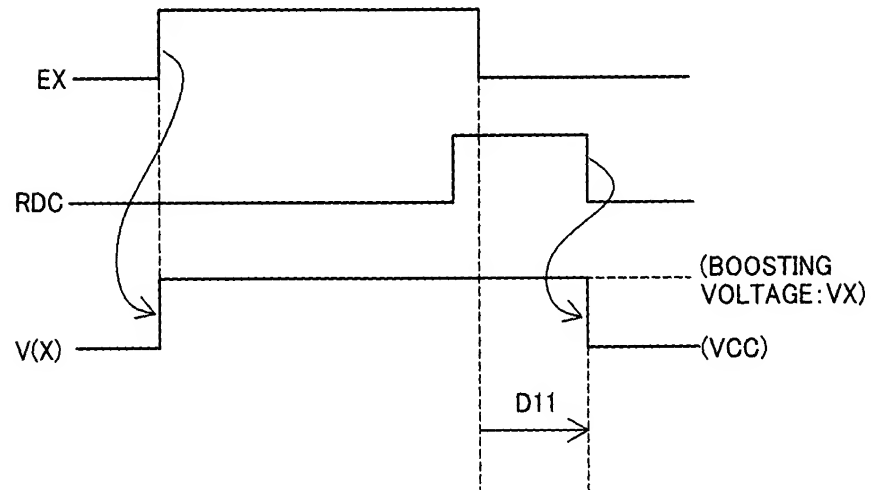
- X: WE**
- WL+ WL-**
- WB**
- n: 0 ~ N**

### CIRCUIT DIAGRAM OF FIRST SPECIFIC EXAMPLE DIRECTED TO FIRST EMBODIMENT



## FIG. 6

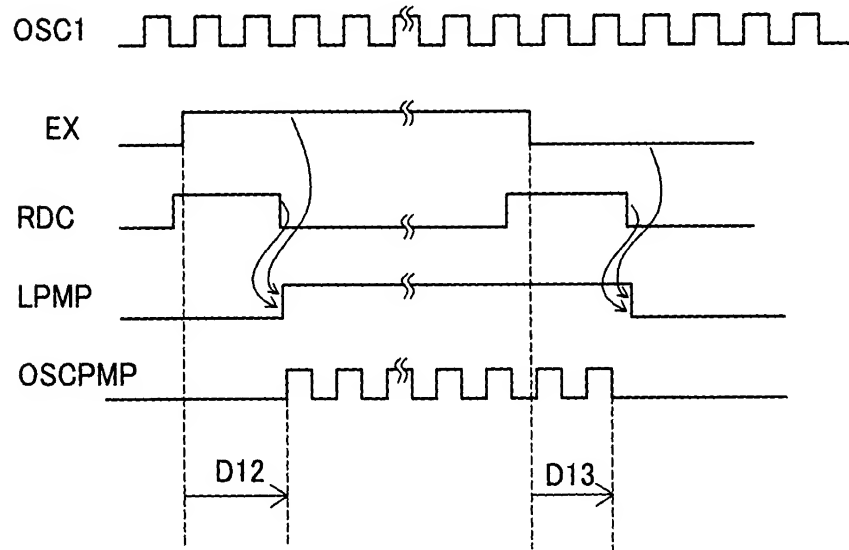
OPERATIONAL WAVEFORM OF FIRST SPECIFIC EXAMPLE  
DIRECTED TO FIRST EMBODIMENT



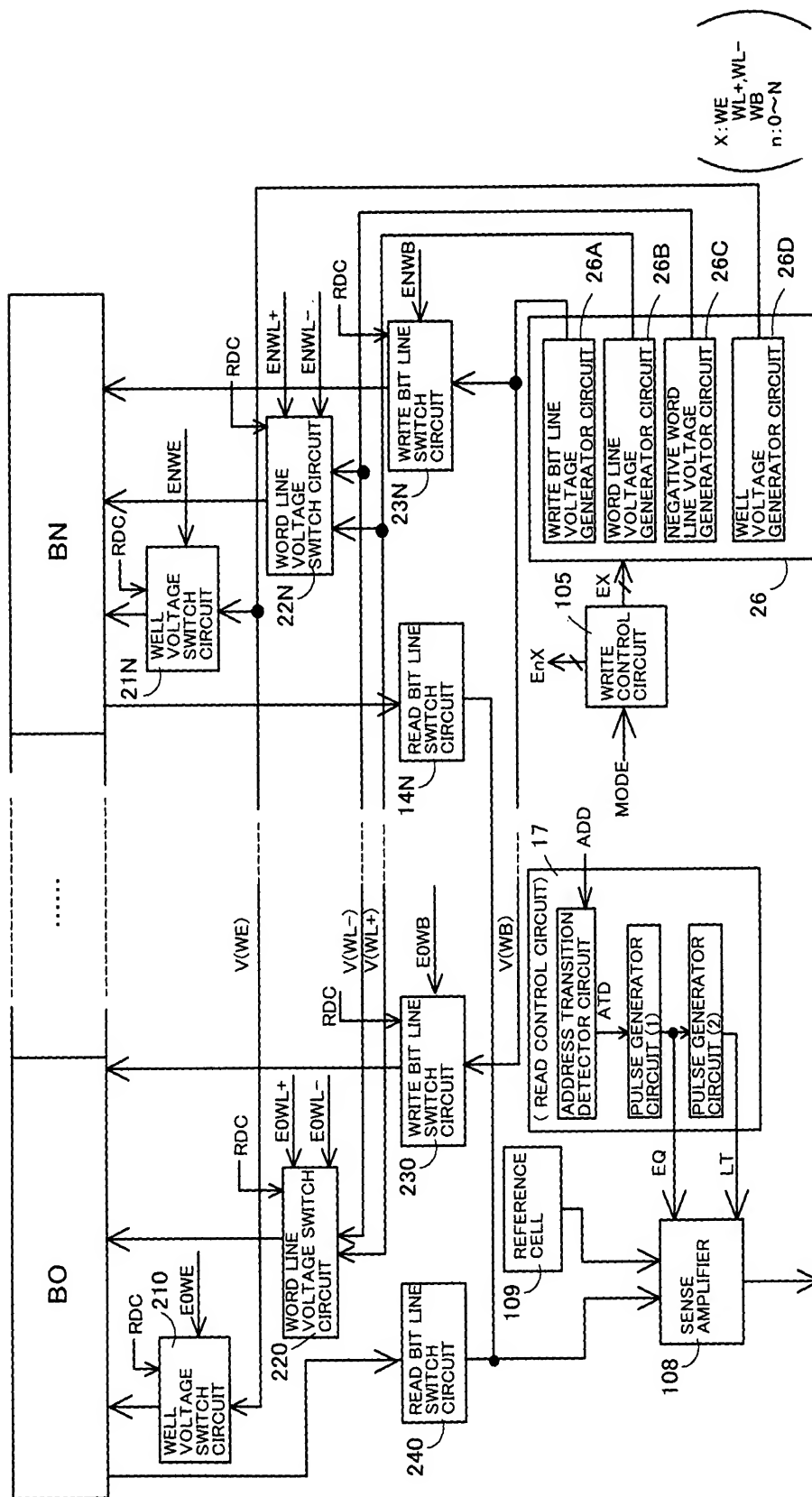


## FIG. 8

OPERATIONAL WAVEFORM OF SECOND SPECIFIC  
EXAMPLE DIRECTED TO FIRST EMBODIMENT



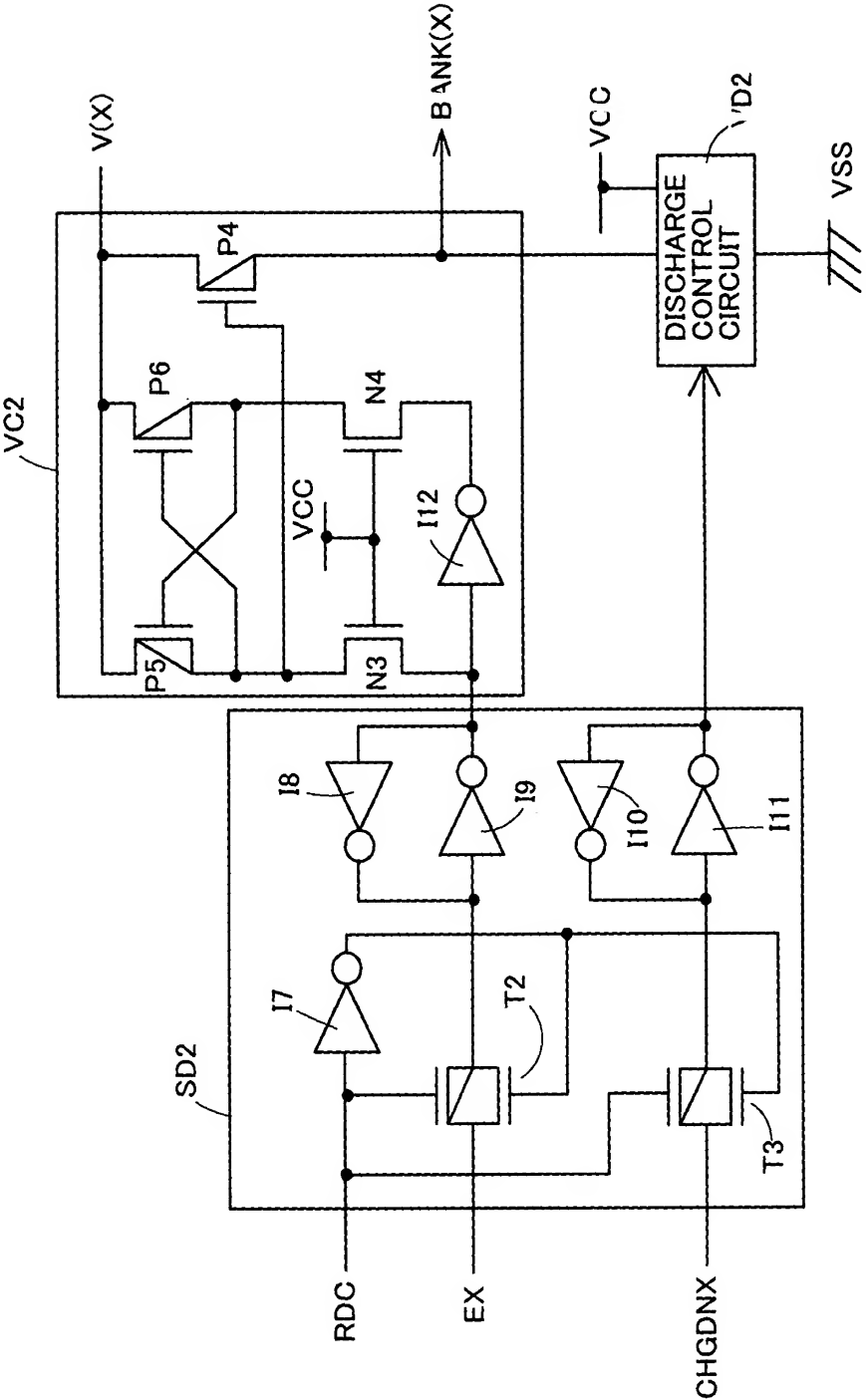
**FIG. 9** CIRCUIT BLOCK DIAGRAM OF SEMICONDUCTOR MEMORY DIRECTED TO SECOND EMBODIMENT



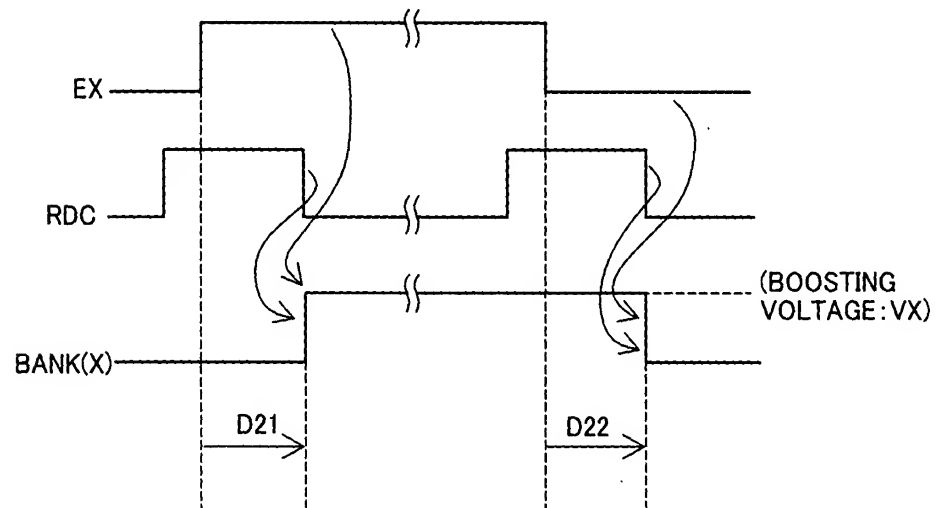
X: WE  
WL+, WL-  
WB  
n: 0 ~ N

FIG. 10

CIRCUIT DIAGRAM OF SPECIFIC EXAMPLE DIRECTED TO SECOND EMBODIMENT



## OPERATIONAL WAVEFORM OF SPECIFIC EXAMPLE DIRECTED TO SECOND EMBODIMENT



**FIG. 12**

**CIRCUIT BLOCK DIAGRAM OF SEMICONDUCTOR MEMORY  
DIRECTED TO THIRD EMBODIMENT**

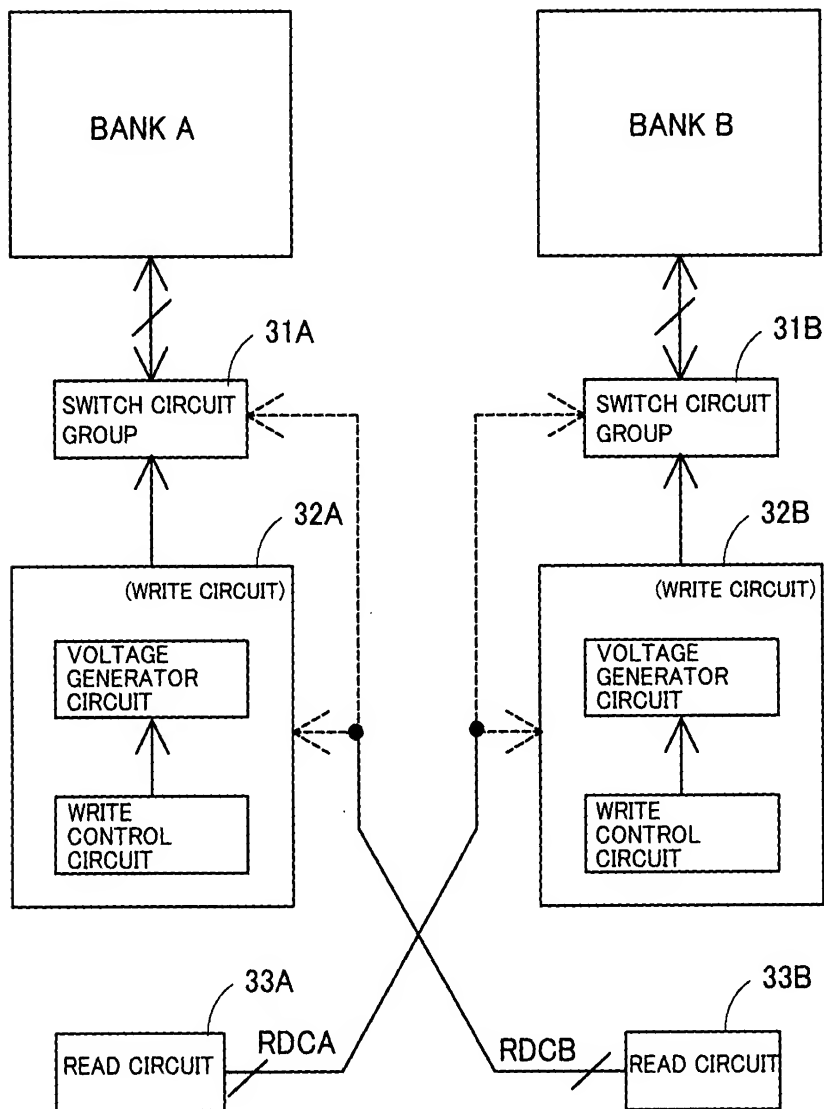
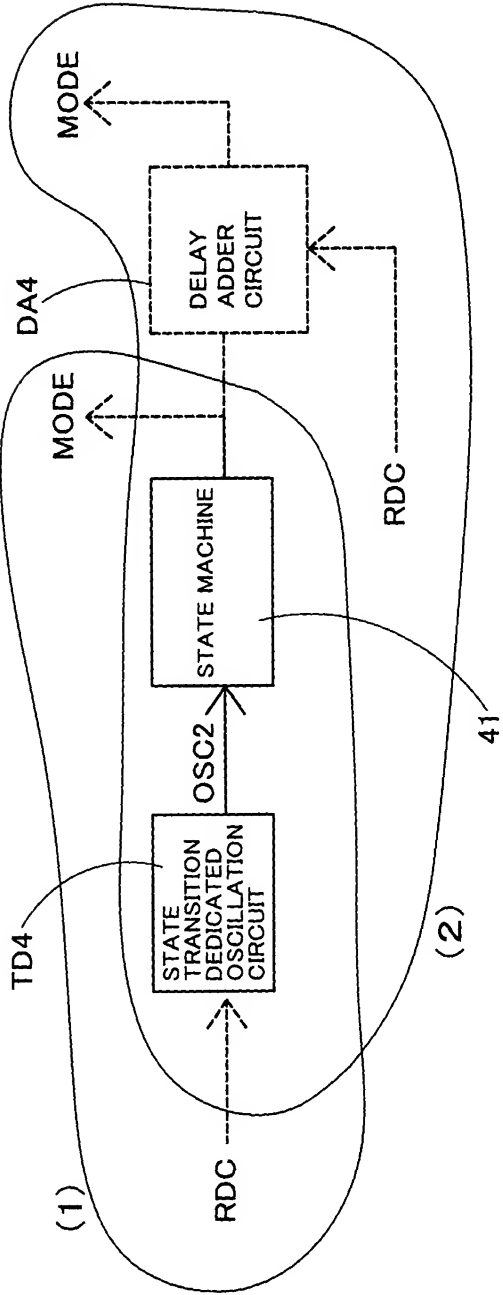


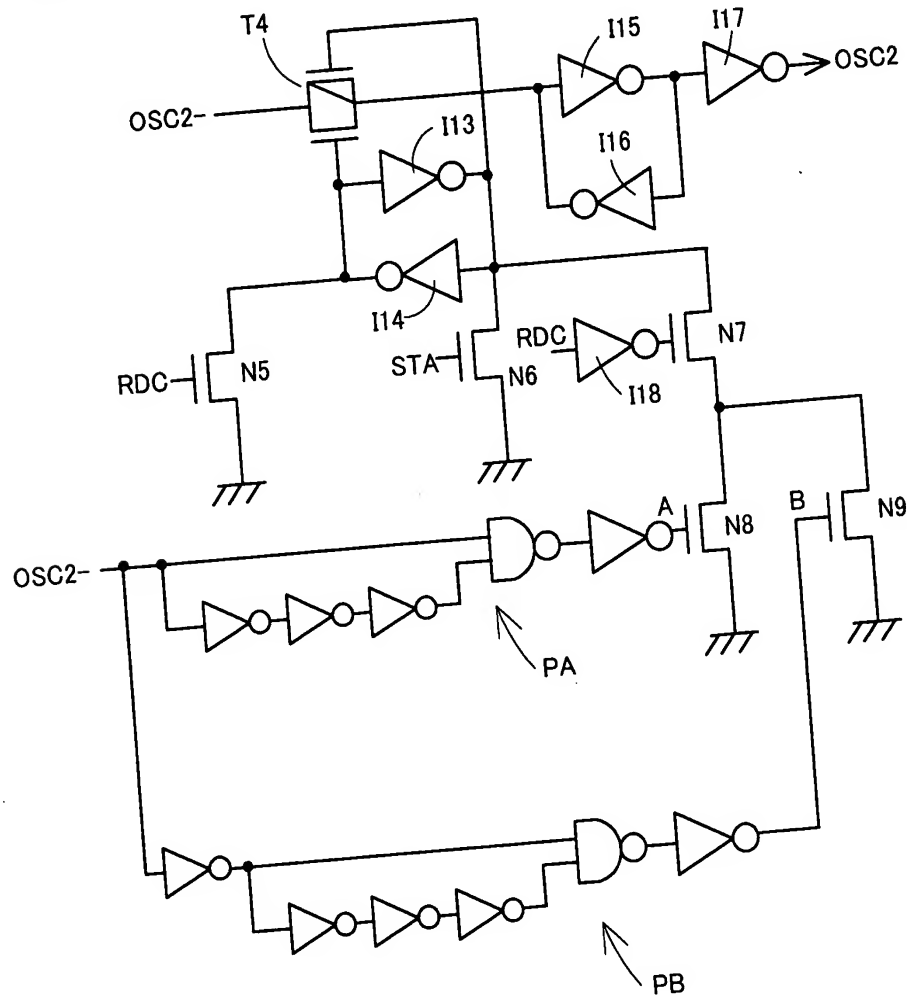
FIG. 13

MODE CONTROL SECTION IN SEMICONDUCTOR MEMORY DIRECTED TO FOURTH EMBODIMENT



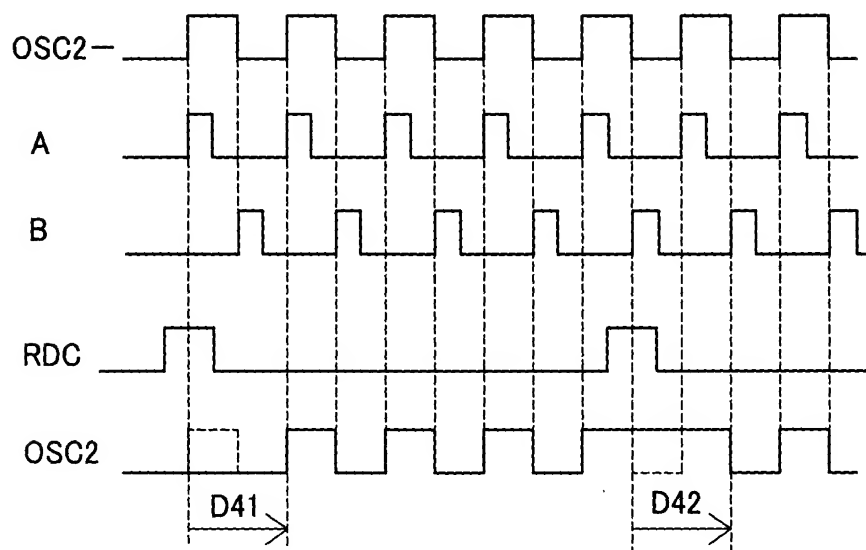
**FIG. 14**

CIRCUIT DIAGRAM OF FIRST SPECIFIC EXAMPLE DIRECTED TO FOURTH EMBODIMENT



## FIG. 15

OPERATIONAL WAVEFORM OF FIRST SPECIFIC EXAMPLE  
DIRECTED TO FOURTH EMBODIMENT



CIRCUIT BLOCK DIAGRAM OF SECOND SPECIFIC EXAMPLE  
DIRECTED TO FOURTH EMBODIMENT

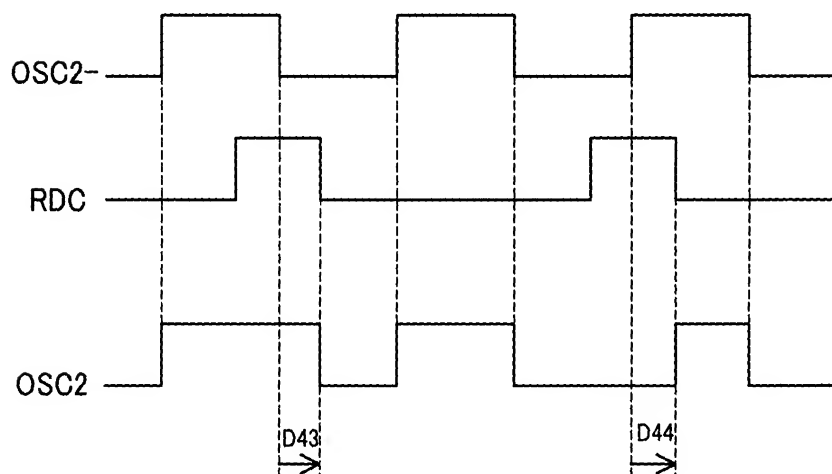


FIG. 18  
CIRCUIT DIAGRAM OF THIRD SPECIFIC EXAMPLE DIRECTED  
TO FOURTH EMBODIMENT



FIG. 15

STATE MACHINE IN SEMICONDUCTOR MEMORY DIRECTED  
TO FIFTH EMBODIMENT

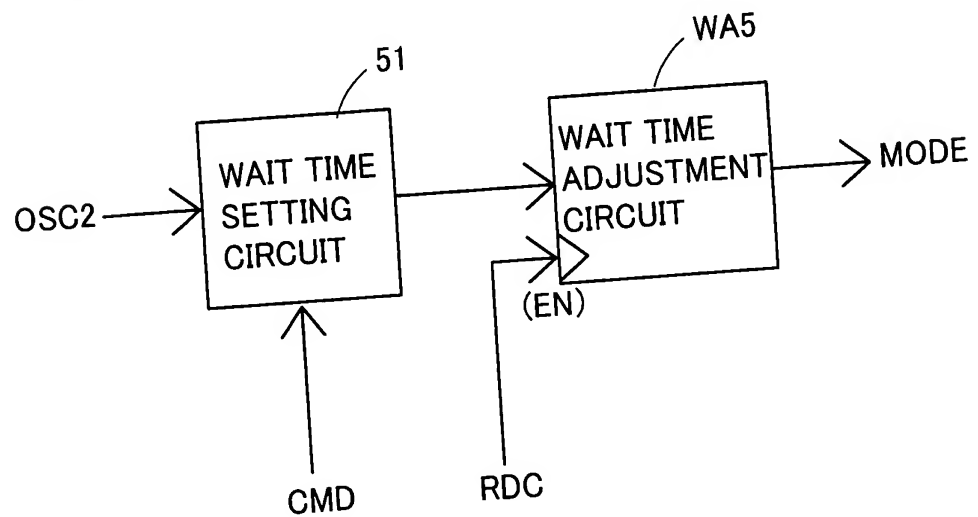
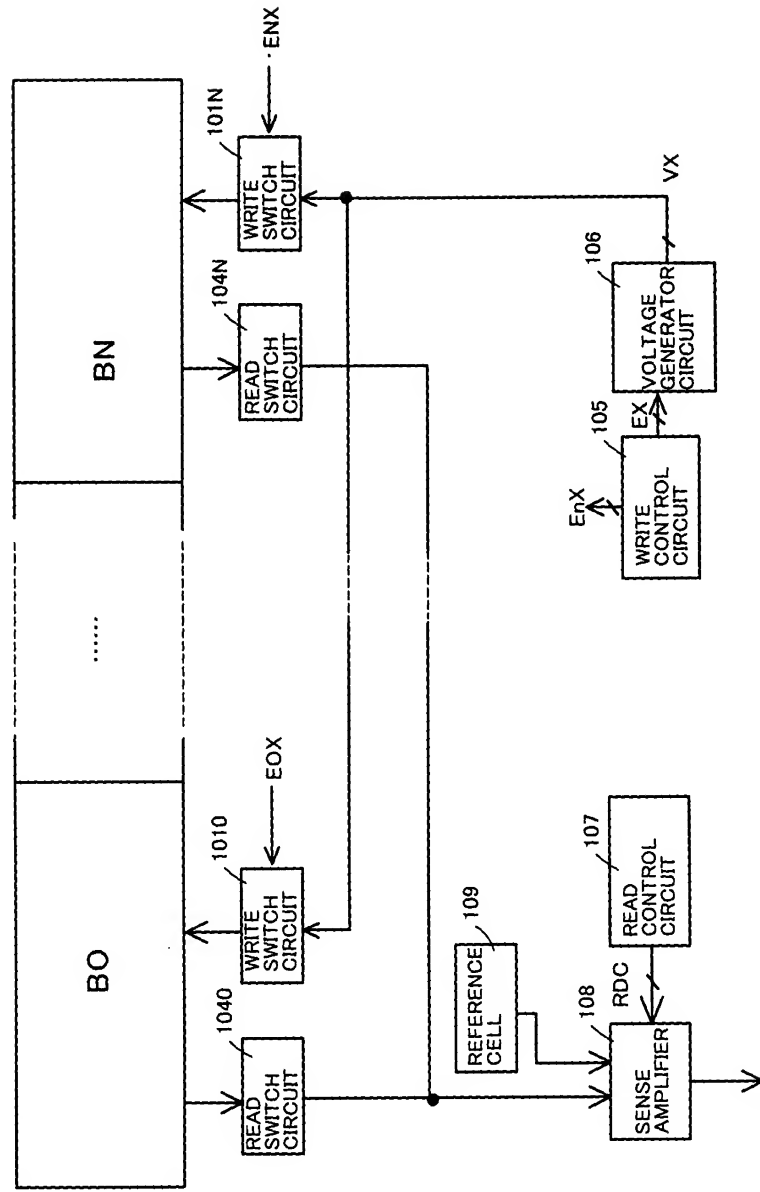


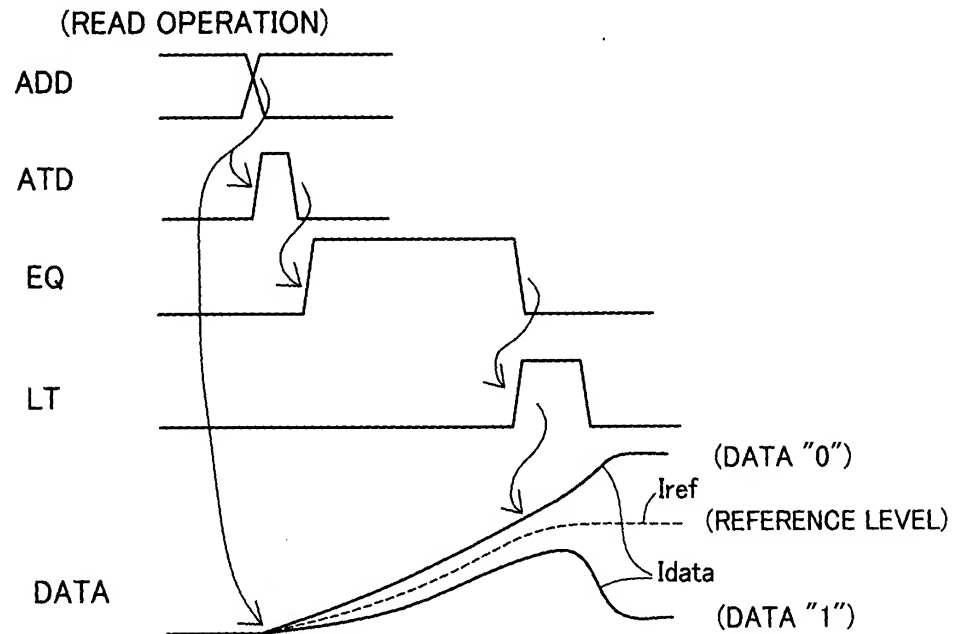
FIG. 20 PRIOR ART

CIRCUIT BLOCK DIAGRAM OF CONVENTIONAL SEMICONDUCTOR MEMORY



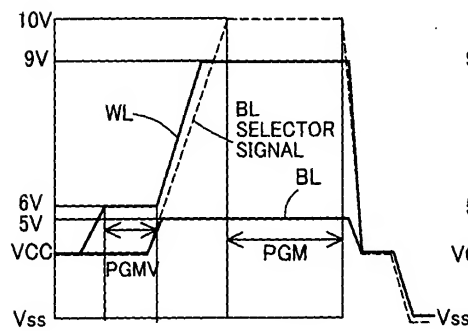
## FIG. 21(A)

### OPERATIONAL WAVEFORM OF RESPECTIVE FUNCTION MODES



## FIG. 21(B)

### (PGM OPERATION)



## FIG. 21(C)

### (ER OPERATION)

